64K x 32
3.3V Synchronous SRAM
Pipelined Outputs
Burst Counter, Single Cycle Deselect

IDT71V632/Z

Features

- **64K x 32 memory configuration**
- **Supports high system speed:**
  Commercial:
  – *A4 4.5ns clock access time (117 MHz)*
  Commercial and Industrial:
  – *5 5ns clock access time (100 MHz)*
  – *6 6ns clock access time (83 MHz)*
  – *7 7ns clock access time (66 MHz)*
- **Single-cycle deselect functionality (Compatible with Micron Part # MT58LC64K32D7LG-XX)**
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **Power down controlled by ZZ input**
- **Operates with a single 3.3V power supply (+10/-5%)**
- **Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP).**

Description

The IDT71V632 is a 3.3V high-speed SRAM organized as 64K x 32 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 117MHz.

The IDT71V632 SRAM contains write, data, address, and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V632 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V632 SRAM utilizes IDT's high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

Pin Description Summary

A_0–A_{15}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chips Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0–I/O_{31}	Data Input/Output	I/O	Synchronous
V_{DD}, V_{DDQ}	3.3V	Power	N/A
V_{SS}, V_{SSQ}	Array Ground, I/O Ground	Power	N/A

3619 tbl 01

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PowerPC is a trademark of International Business Machines, Inc.

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

3619 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD}, V_{DDQ} and Input terminals only.
3. I/O terminals.

Capacitance
(T_A = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3619 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V+10/-5%	3.3V+10/-5%
Industrial	–40°C to +85°C	0V	3.3V+10/-5%	3.3V+10/-5%

3619 tbl 03

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.63	V
V_{DDQ}	I/O Supply Voltage	3.135	3.63	V
V_{SS}, V_{SSQ}	Ground	0	0	V
V_{IH}	Input High Voltage — Inputs	2.0	5.0(1)	V
V_{IH}	Input High Voltage — I/O	2.0	V_{DDQ}+0.3(2)	V
V_{IL}	Input Low Voltage	–0.3(3)	0.8	V

3619 tbl 04

NOTES:
1. V_{IH} (max) = 6.0V for pulse width less than t_{CYC}/2, once per cycle.
2. V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than t_{CYC}/2, once per cycle.
3. V_{IL} (min) = –1.0V for pulse width less than t_{CYC}/2, once per cycle.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +10/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LZZ}\|$	ZZ and $\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL} (3.3V)	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage	I_{OH} = –5mA, V_{DD} = Min.	2.4	—	V

NOTE: 3619 tbl 12

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) (V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Conditions	SA4(3,4)		S5		S6		S7		Unit
			Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	220	—	200	200	180	180	160	160	mA
I_{SB}	Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	70	—	65	65	60	60	55	55	mA
I_{SB1}	Full Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2)	15	—	15	15	15	15	15	15	mA
I_{ZZ}	Full Sleep Mode Power Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	10	—	10	10	10	10	10	10	mA

NOTES: 3619 tbl 13

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. SA4 speed grade corresponds to a t_{CD} of 4.5 ns.
4. 0°C to +70°C temperature range only.

AC Test Loads

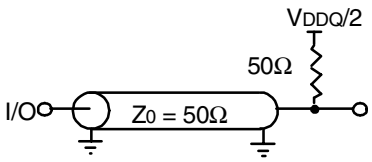
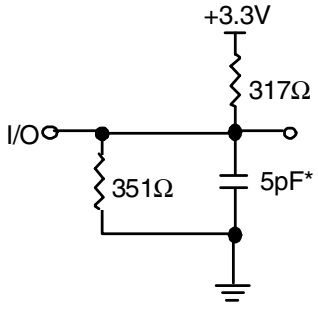
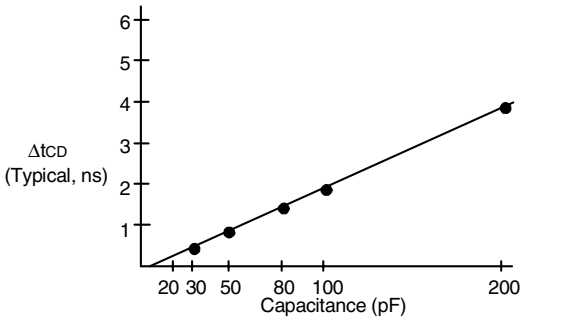


Figure 1. AC Test Load 3619 drw 03



* Including scope and jig capacitance. 3619 drw 04

Figure 2. High-Impedence Test Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})



3619 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3619 tbl 14

AC Electrical Characteristics

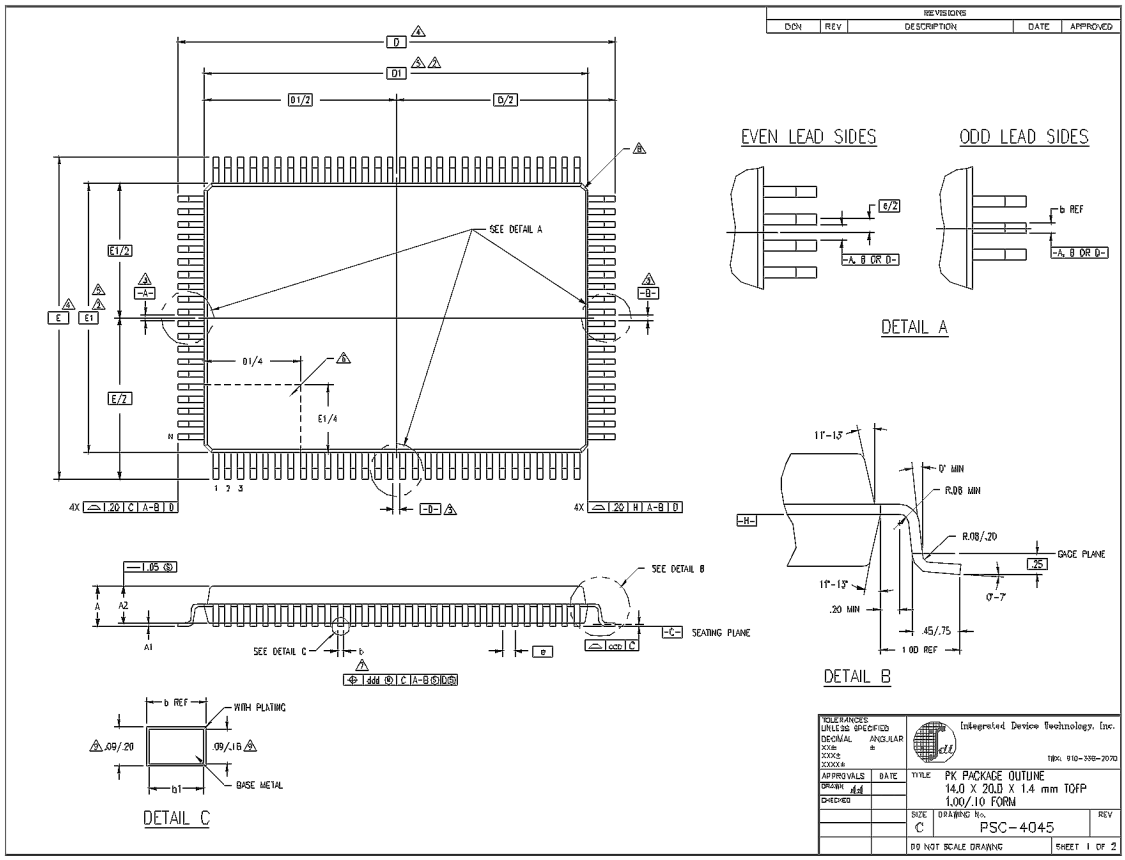
(VDD, VDDQ = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)

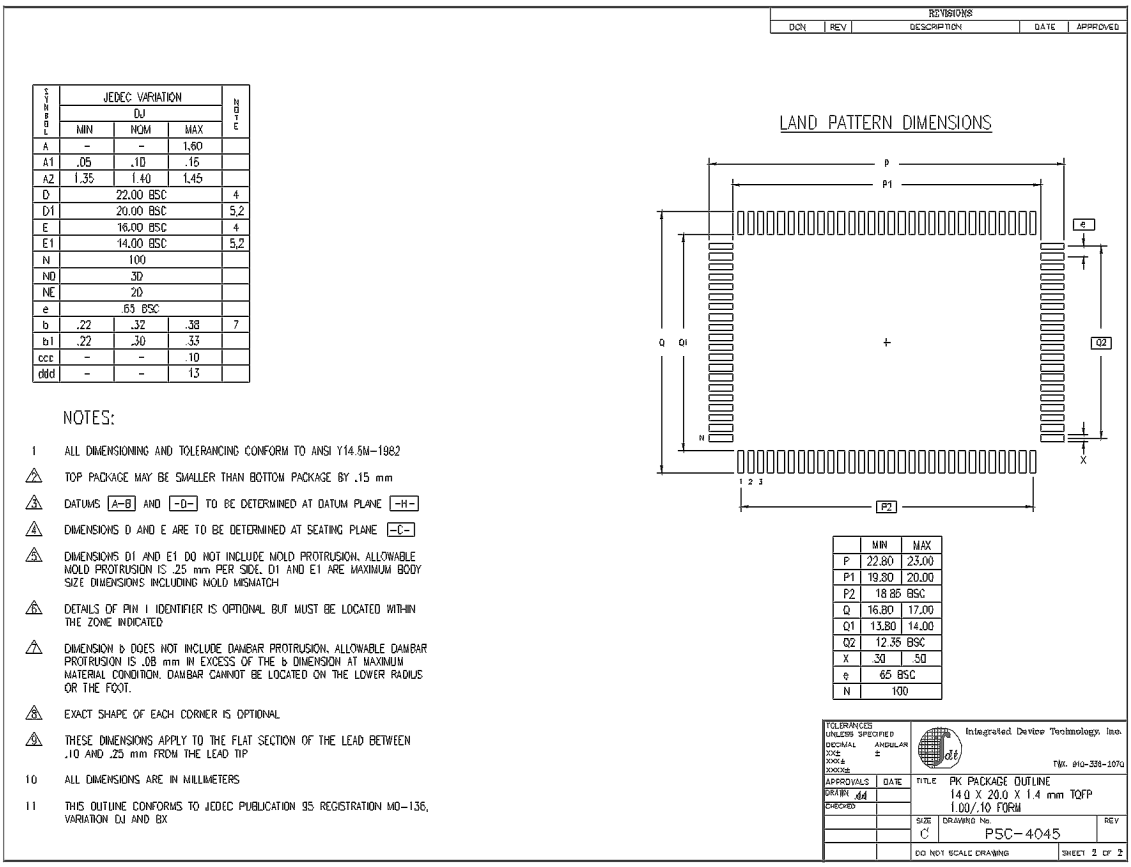
Symbol	Parameter	71V632SA4[5,6]		71V632S5		71V632S6		71V632S7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CLOCK PARAMETERS										
t_{CYC}	Clock Cycle Time	8.5	—	10	—	12	—	15	—	ns
t_{CH}[1]	Clock High Pulse Width	3.5	—	4	—	4.5	—	5	—	ns
t_{CL}[1]	Clock Low Pulse Width	3.5	—	4	—	4.5	—	5	—	ns
OUTPUT PARAMETERS										
t_{CD}	Clock High to Valid Data	—	4.5	—	5	—	6	—	7	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	2	—	2	—	ns
t_{CLZ}[2]	Clock High to Output Active	0	—	0	—	0	—	0	—	ns
t_{CHZ}[2]	Clock High to Data High-Z	1.5	4	1.5	5	2	5	2	6	ns
t_{OE}	Output Enable Access Time	—	4	—	5	—	5	—	6	ns
t_{OLZ}[2]	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Enable High to Data High-Z	—	4	—	4	—	5	—	6	ns
SETUP TIMES										
t_{SA}	Address Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
t_{SS}	Address Status Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
t_{SD}	Data in Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
t_{SW}	Write Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
t_{SAV}	Address Advance Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	2.2	—	2.5	—	2.5	—	2.5	—	ns
HOLD TIMES										
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
SLEEP MODE AND CONFIGURATION PARAMETERS										
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	100	—	ns
t_{ZZR}[3]	ZZ Recovery Time	100	—	100	—	100	—	100	—	ns
t_{CFG}[4]	Configuration Set-up Time	34	—	40	—	50	—	50	—	ns

3619 tbl 15

NOTES:
1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.
5. The 71V632SA4 speed grade corresponds to a t_{CD} of 4.5ns.
6. 0°C to +70°C temperature range only.

100-pin Thin Quad Plastic Flatpack (TQFP) Package Diagram Outline





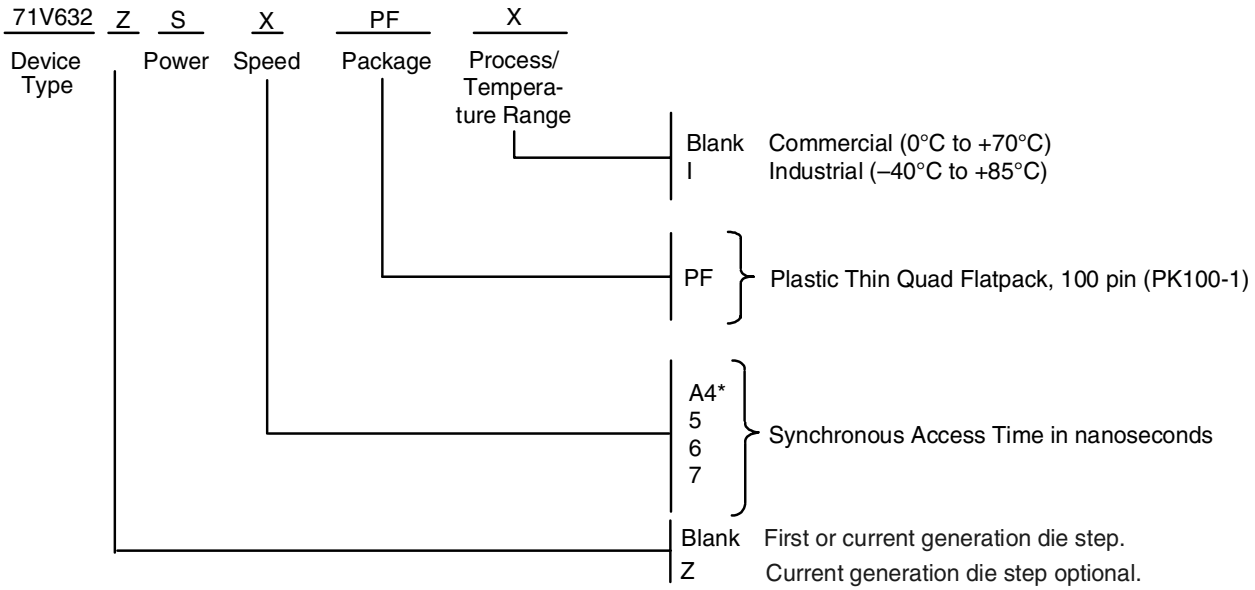
SYMBOL	JEDEC VARIATION DJ MIN	DJ NOM	DJ MAX	NOTE
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			4
D1	20.00 BSC			5,2
E	16.00 BSC			4
E1	14.00 BSC			5,2
N	100			
ND	30			
NE	20			
e	.65 BSC			
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–136, VARIATION DJ AND BX

	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

Ordering Information



* Commercial only.

PART NUMBER	SPEED IN MEGAHERTZ	tCD PARAMETER	CLOCK CYCLE TIME
71V632SA4PF	117 MHz	4.5 ns	8.5 ns
71V632S5PF	100 MHz	5 ns	10 ns
71V632S6PF	83 MHz	6 ns	12 ns
71V632S7PF	66 MHz	7 ns	15 ns

3619 drw 13